REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of June 7, 2006 (hereinafter "Office Action"). Applicants especially appreciate the indication that Claims 2 - 6, 9 - 13, 15 - 18, and 20 - 24 recite patentable subject matter. Rather than writing any of the allowable claims in independent form at this time, Applicants respectfully submit that the cited references do not disclose or suggest all of the recitations of the independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1, 14, 19 are Patentable

Independent Claims 1, 14, and 19 stand rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 5,329,251 to Llewellyn (hereinafter "Llewellyn"). (Office Action, page 2).

Independent Claim 1 is directed to a clock distribution circuit and includes the following recitations:

> a first clock circuit that is configured to generate a first clock signal responsive to an error signal;
> a second clock circuit that is configured to generate a second clock signal responsive to the error signal; and
> a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals.

Independent Claims 14 and 19 include similar recitations. Thus, independent Claims 1, 14, and 19 all include recitations that indicate that the first and second clock circuits generate respective clock signals responsive to the same error signal, which is generated by a phase detector circuit that connects the first and second clock circuits.

In rejecting Claims 1, 14, and 19, the Office Action cites passages from the Summary section of Llewellyn without identifying the specific elements in Llewellyn that are alleged to correspond go the specific recitations of independent Claims 1, 14, and 19. (Office Action,

pages 2 - 3). Nevertheless, Applicants will show below that none of the circuits discussed in Llewellyn disclose the specific combinations of elements recited in independent Claims 1, 14, and 19.

Llewellyn illustrates three circuits in FIGS. 3 - 5, respectively, that have similar architectures. Accordingly, while Applicants' analysis herein is directed to the circuit of FIG. 3, the analysis is similarly applicable to FIGS. 4 and 5. The circuit shown in FIG. 3 of Llewellyn includes three circuits: a PLL clock circuit that includes the digital processor 112, DAC 134, and CCO 132, a first PLL circuit 122, and a second PLL circuit 116. PLL circuits 116 and 122 are similar to each other and are each connected to the PLL clock circuit via a multiplexer 130. Applicants submit that the first PLL circuit 122 and second PLL circuit 116 do not correspond to the first and second clock circuits recited in independent Claims 1, 14, and 19 because their output signals are each generated responsive to **different** error signals. In the case of the first PLL circuit 122, the output signal V_{OSCT} is generated in response to an error signal that represents a difference between the output signal V_{OSCT} and an input signal V_{ETB}. In the case of the second PLL circuit 116, the output signal V_{OSCB} is generated in response to an error signal that represents a difference between the output signal V_{OSCB} and an input signal V_{EBB}.

Applicants further submit that the PLL clock circuit, including digital processor 112, DAC 134, and CCO 132 and either of the first and second PLL circuits 122 and 116 do not correspond to the first and second clock circuits recited in independent Claims 1, 14, and 19. Using the first PLL circuit 122 as an example, the clock signal RCLK output from CCO 132 and the output signal V_{OSCT} output from the CCO 124 are both generated responsive to the error signal output from the phase detector 126. The output signal V_{OSCT} is not, however, generated responsive to the Digital Error Word (DEW) generated by the digital processor 112; therefore, the phase detector 126 of the first PLL circuit 122 is the only component that could correspond to the phase detector circuit recited in Claim 1, for example.

Claim 1 includes the following recitation directed to the phase detector circuit:

> a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive

to the first and the second clock signals.

Claim 14 includes the following recitation directed to generating the error signal:

> generating the error signal based on a relative phase difference between the first clock signal and the second clock signal.

Independent Claim 19 includes recitations similar to Claim 14.

With respect to Claim 1, the phase detector circuit is described as connecting the first and second clock circuits. Applicants submit that the phase detector 126 of Llewellyn does not connect the PLL clock circuit, which includes the digital processor 112, the DAC 134, and the CCO 132, to the first PLL circuit 122. Moreover, with respect to Claims 1, 14, and 19, the error signal is described as being generated responsive to the first and second clock signals. Applicants submit that the error signal output from the phase detector 126 of Llewellyn is not generated responsive to the clock signal RCLK output from the PLL clock circuit and the output signal V_{OSCT} output from the first PLL circuit 122, but is instead generated responsive to the output signal V_{OSCT} and input signal V_{ETB}.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 14, and 19 are patentable over the cited reference and that Claims 2 - 7, 15 - 18, and 20 - 24 are patentable at least per the patentability of independent Claims 1, 14, and 19.

Independent Claim 8 is Patentable

Independent Claim 8 stands rejected under 35 U.S.C. §102(b) as being anticipated by Llewellyn. Independent Claim 8 is directed to a clock distribution circuit that comprises a plurality of clock circuits that are responsive to respective ones of a plurality of error signals that are generated by respective ones of a plurality of phase detector circuits that directly connect respective ones of the plurality of clock circuits to one or more other ones of the clock circuits as indicated by the recitations of Claim 8 reproduced in part below:

> ...
> a plurality of clock circuits, respective ones of the plurality of clock

> circuits being directly connected to at least one other of the plurality of clock circuits by respective ones of the plurality of phase detector circuits, respective ones of the plurality of phase detector circuits being configured to generate respective ones of a plurality of error signals responsive to respective ones of a plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected thereby, the respective ones of the plurality of clock circuits being configured to generate respective ones of the plurality of clock signals responsive to respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits. (Emphasis added)

According to Claim 8, respective ones of the phase detectors generate respective ones of the error signals in response to clock signals generated by clock circuits that are directly connected by respective ones of the phase detectors.

Applicants respectfully submit that Claim 8 is patentable over Llewellyn for at least the same reasons discussed above with respect to independent Claims 1, 14, and 19. That is, the phase detector 126 of Llewellyn does not connect the PLL clock circuit, which includes the digital processor 112, the DAC 134, and the CCO 132, to the first PLL circuit 122. Moreover, the error signal output from the phase detector 126 of Llewellyn is **not** generated responsive to the clock signal RCLK output from the PLL clock circuit and the output signal V_{OSCT} output from the first PLL circuit 122, but is instead generated responsive to the output signal V_{OSCT} and input clock signal V_{ETB}.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 8 is patentable over the cited reference and that Claims 9 - 13 are patentable at least per the patentability of independent Claim 8.

Independent Claims 25 and 26 Are Patentable

Independent Claims 25 and 26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Llewellyn. Independent Claim 25 is directed to a method of distributing a clock signal and recites, in part:

...

synchronizing phases of the plurality of clock signals to one another based on error signals that are generated based on relative phase differences between ones of the plurality of clock signals.

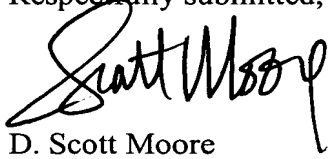
Independent Claim 26 includes similar recitations. Thus, according to independent Claims 25 and 26, the clock signals are synchronized to one another based on error signals corresponding to phase differences between the clock signals. As discussed above with respect to independent Claims 1, 8, 14, and 19, the error signal output from the phase detector 126 of Llewellyn is **not** generated responsive to the clock signal RCLK output from the PLL clock circuit and the output signal V_{OSCT} output from the first PLL circuit 122, but is instead generated responsive to the output signal V_{OSCT} and input signal V_{ETB}. Applicants submit, therefore, that Llewellyn does not teach synchronization of clock signals to one another based on error signals corresponding to phase differences between the clock signals.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 25 and 26 are patentable over Llewellyn.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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